Invitation to January 25, 2010 IEEE/LVS/SSCS Technical Meeting

Featuring: **K. R. (Kumar) Lakshmikumar**
Topic: **PLL Design in Nanometer CMOS**

When?
Monday, January 25, 2010, beginning at 6:00 PM

Where?
Lehigh University, Bethlehem PA
Packard Laboratory
Refreshments in room 324 (Same floor as the lobby)
Meeting and lecture upstairs in room 416.

Who is invited?
Basically anybody who's interested may attend ***as long as they RSVP***, but specific invitations will be extended to:

- IEEE/LVS members (not just SSCS)
- IEEE/LVS student branch members
- Lehigh University Professors and Students
- IEEE/SSCS of neighboring sections
- Local industry engineers and managers, IEEE members or not

Program
6:00 PM Social Hour in Packard Lab room 324. RSVP is strictly required to partake of Pizza, Soft Drinks and Cookies.
7:00 PM Announcements and short formal meeting, followed by address by Dr. Kumar Lakshmikumar of Ikanos Communications, Red Bank, NJ.

Topic
PLL Design in Nanometer CMOS. Kumar's talk is a preview of the PLL tutorial he is presenting at the 2010 ISSCC and a wonderful opportunity for those of us unable to attend the ISSCC this year.

Abstract
A PLL is perhaps the most widely used mixed-signal circuit block in a system-on-chip (SoC). Advancements in process technology offer advantages as well as challenges for the design of PLLs. This tutorial will highlight the challenges and present design techniques to overcome them. A brief discussion of PLL basics is presented first. Noise transfer functions from various points in the loop to the output are shown and the importance of having a low oscillator-gain is highlighted. Optimization of loop parameters to minimize phase-noise and area is emphasized. Challenges posed by nanometer CMOS technology are then discussed. Circuit techniques to overcome these are discussed for critical building blocks. Process and temperature compensation techniques to minimize VCO gain, capacitance multiplication techniques to minimize loop-filter area, and a rail-to-rail output swing charge-pump with matched up/down currents to minimize spurs are a few of the circuit techniques that will be discussed.

Speaker Information

K. R. (Kumar) Lakshmikumar received the Ph.D., in Electrical Engineering from Carleton University, Ottawa, Canada in 1985. He has been making significant contributions to many aspects of mixed-signal design such as, system design, chip-architecture, circuit design, characterization and testing, and introduction to manufacture. These designs address diverse applications such as, cellular telephony, serial data transceivers, and DSL systems. He has held senior engineering and management positions at Bell Labs, Multilink and Conexant Systems. He is currently with Ikanos Communications, Red Bank, NJ. He has many patents and papers to his credit. His paper on MOS device matching in the December 1986 issue of IEEE Journal of Solid-State Circuits is among the top 20 most referenced papers published by the journal between 1968 and 1992.